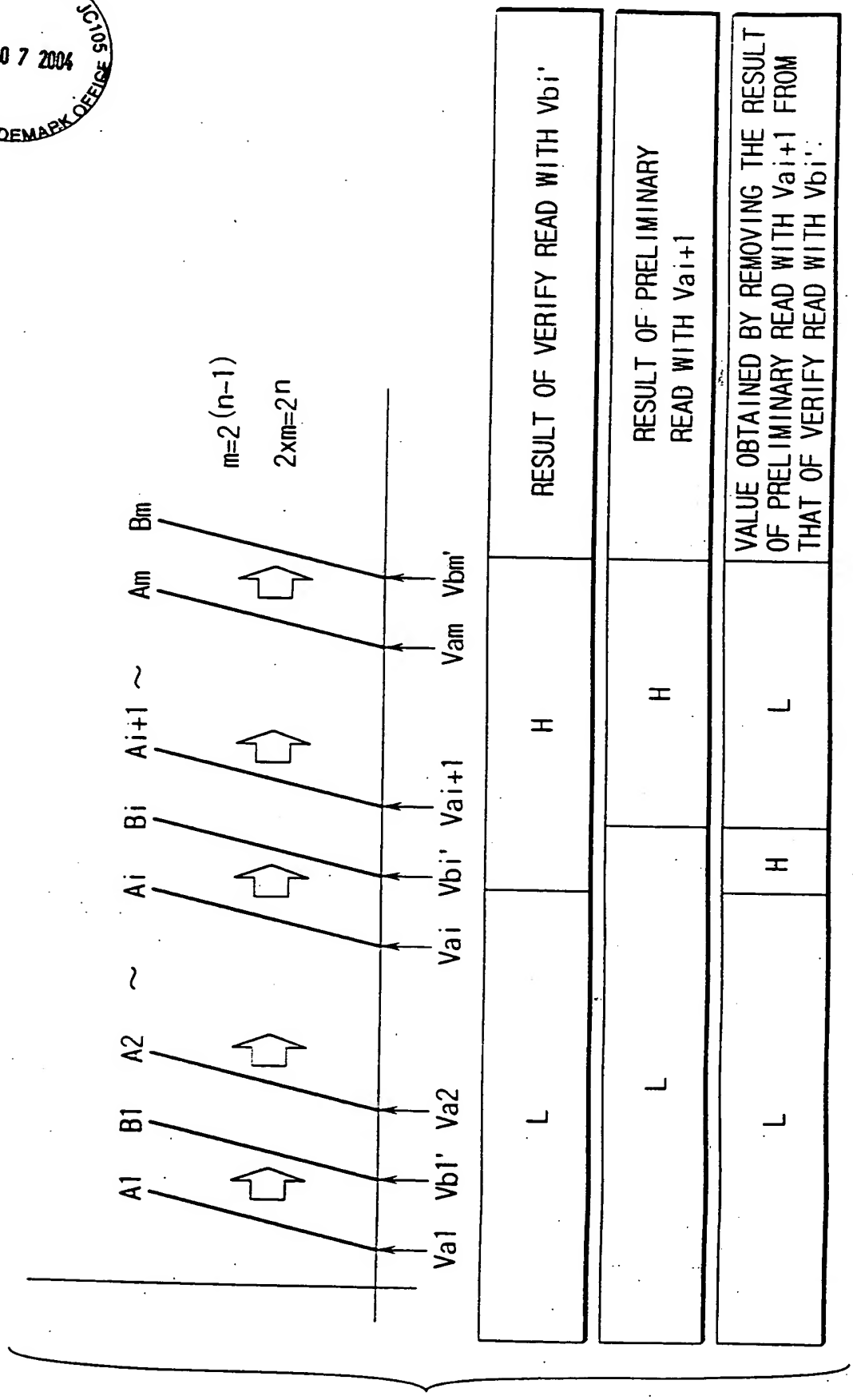


FIG. 1

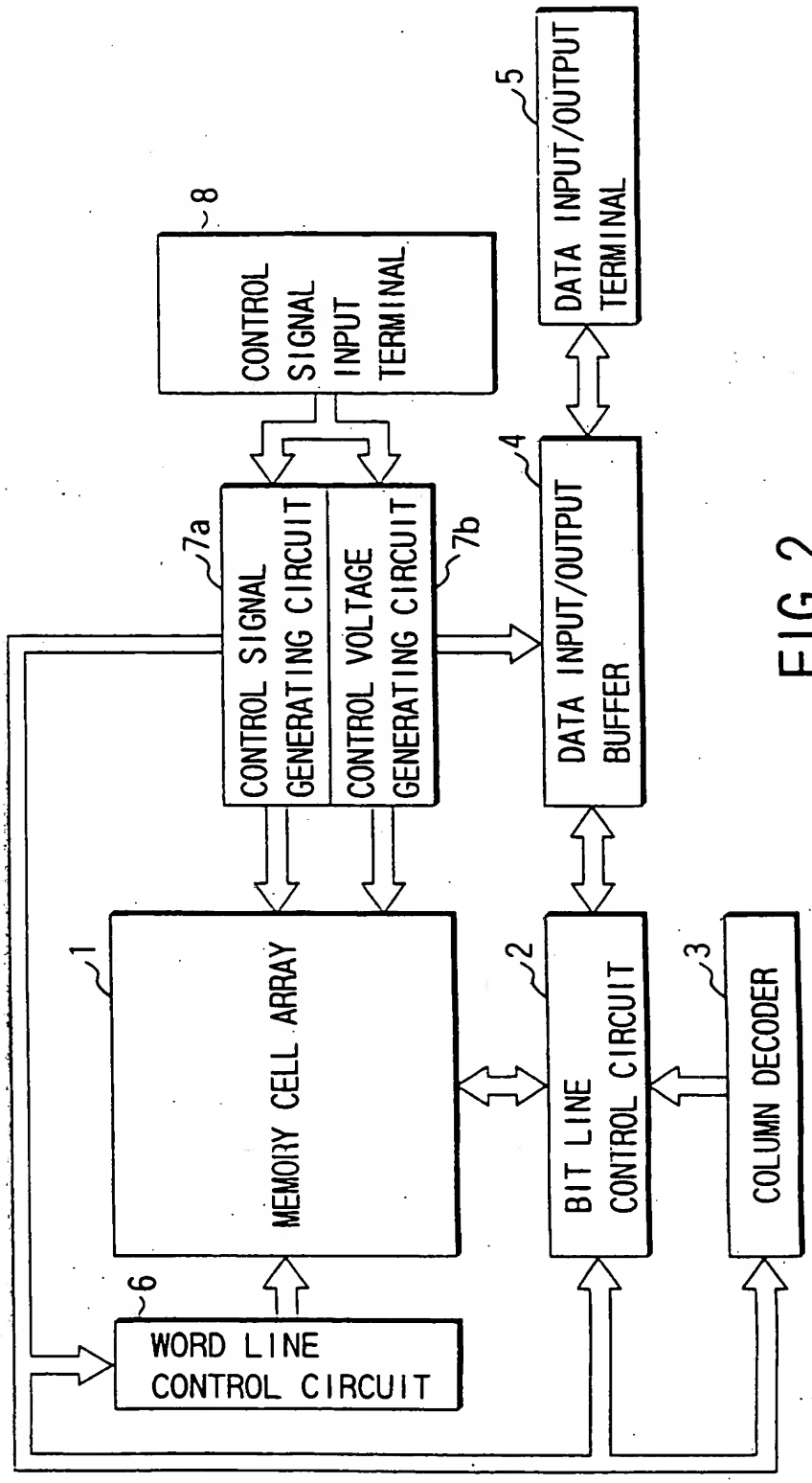

8
CONTROL SIGNAL INPUT TERMINAL
5
DATA INPUT/OUTPUT TERMINAL
7a
CONTROL SIGNAL GENERATING CIRCUIT
7b
CONTROL VOLTAGE GENERATING CIRCUIT
4
DATA INPUT/OUTPUT BUFFER
1
MEMORY CELL ARRAY
2
BIT LINE CONTROL CIRCUIT
3
COLUMN DECODER
6
WORD LINE CONTROL CIRCUIT

FIG. 2

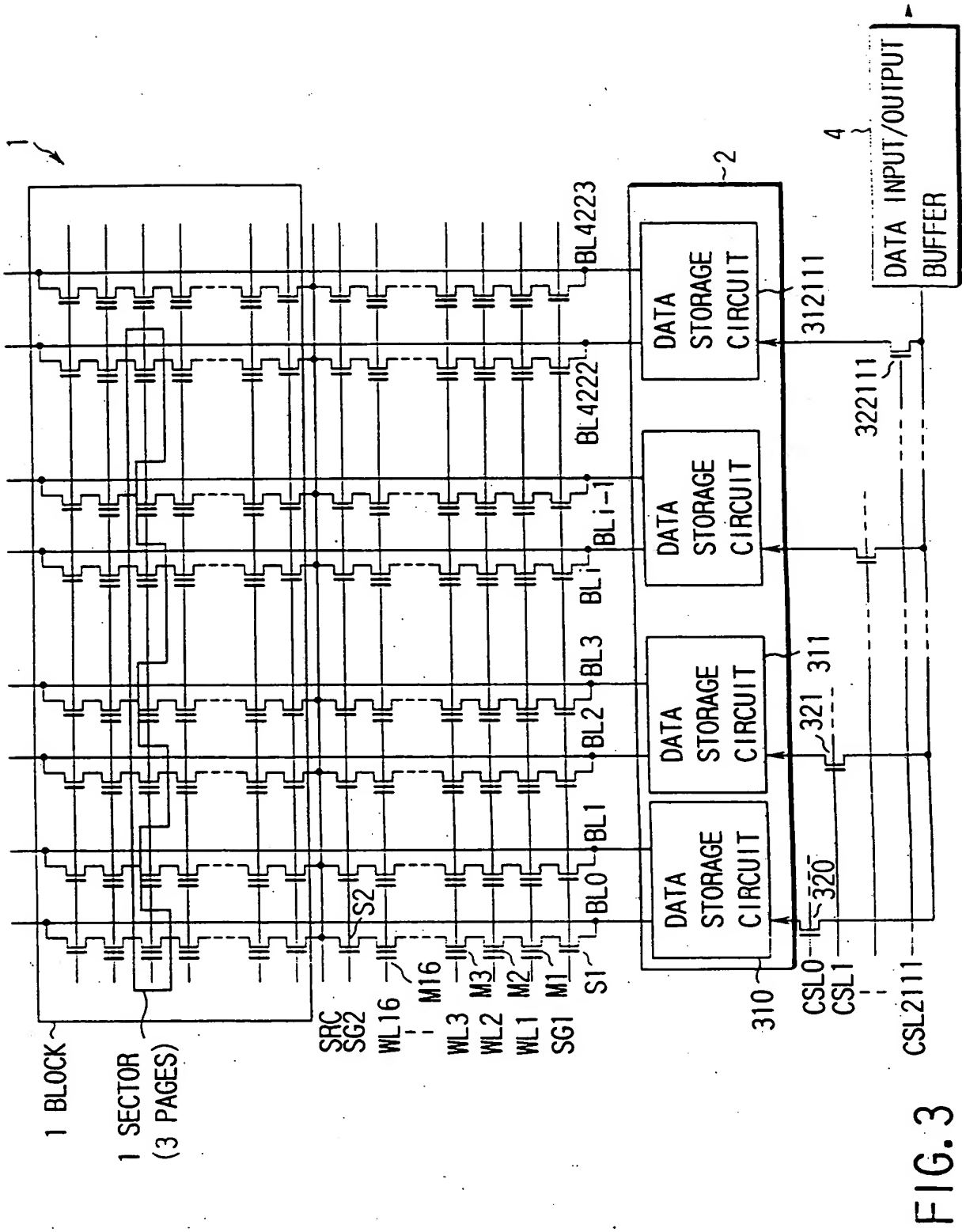

1
2
4
DATA INPUT/OUTPUT BUFFER
DATA STORAGE CIRCUIT
312111
322111
321
311
320
310
CSL0
CSL1
CSL2111
BL4223
BL4222
BLi-1
BLi
BL3
BL2
BL1
BL0
S1
S2
SRC
SG2
WL16
M16
WL3
M3
WL2
M2
WL1
M1
SG1
1 BLOCK
1 SECTOR
(3 PAGES)

FIG. 3

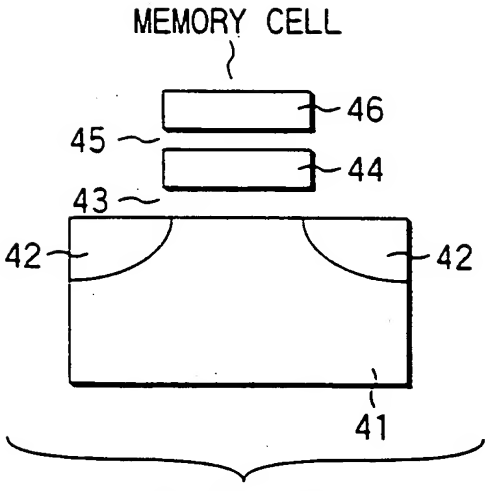


FIG. 4A

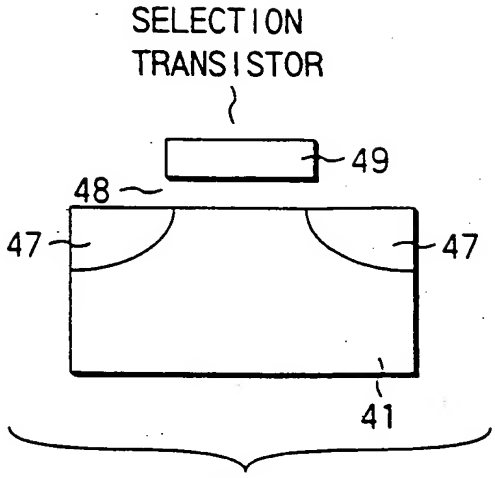


FIG. 4B

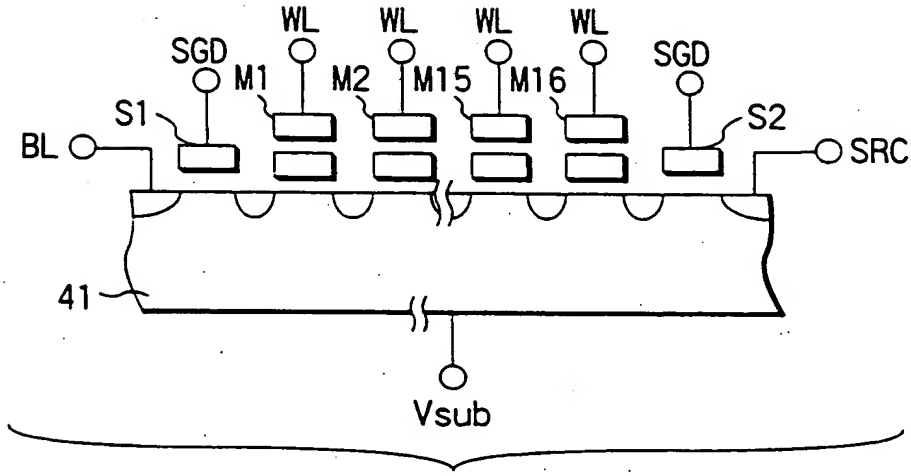


FIG. 5

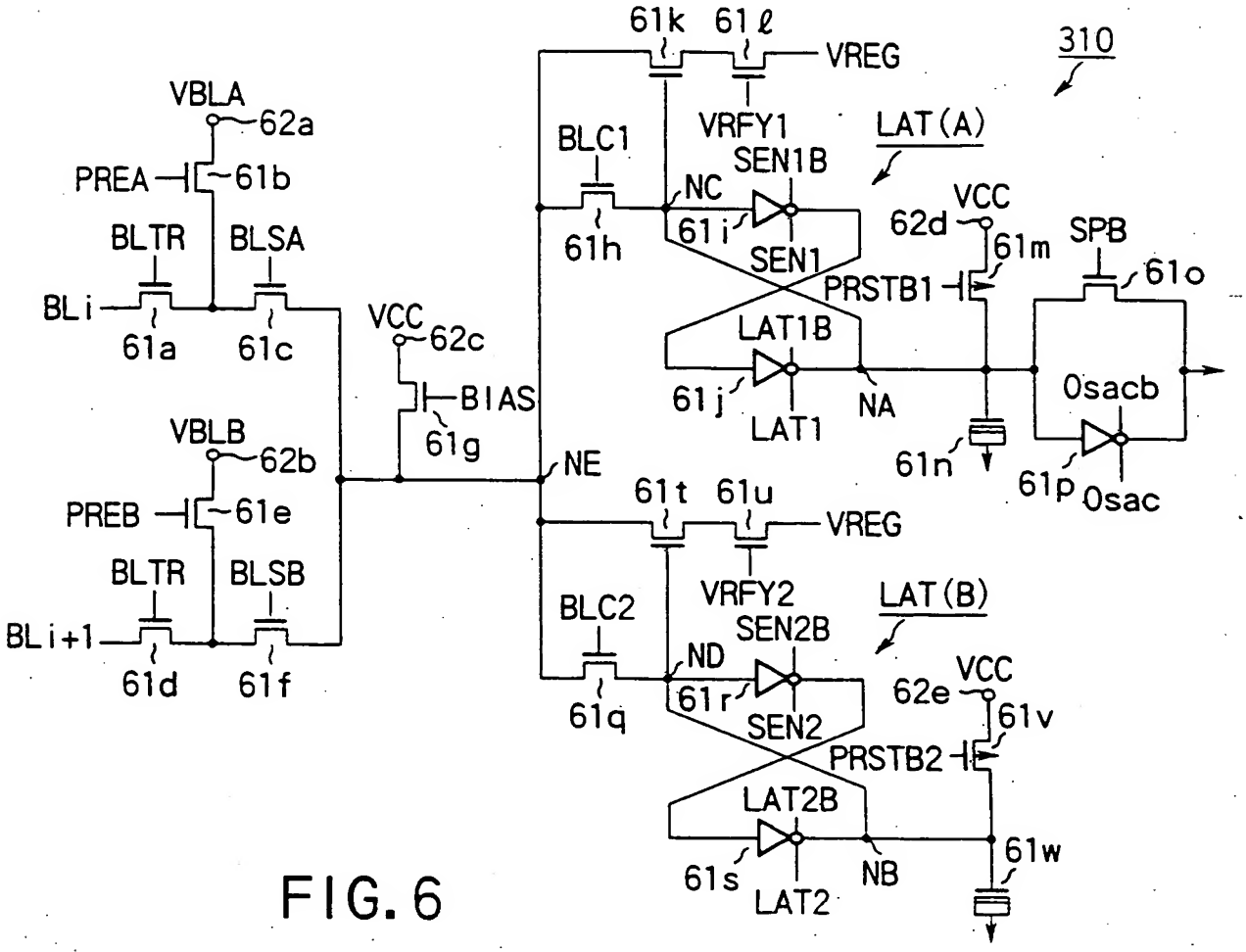

61k
61ℓ
VREG
310
VBLA
62a
PREA
61b
BLTR
BLSA
BLi
61a
61c
VCC
62c
BIAS
61g
VBLB
62b
PREB
61e
BLTR
BLSB
BLi+1
61d
61f
NE
BLC1
61h
VRFY1
SEN1B
LAT(A)
NC
61i
SEN1
VCC
62d
61m
SPB
61o
PRSTB1
LAT1B
61j
LAT1
NA
Osacb
61n
61p
Osac
61t
61u
VREG
BLC2
61q
VRFY2
SEN2B
LAT(B)
ND
61r
SEN2
VCC
62e
61v
PRSTB2
LAT2B
61s
LAT2
NB
61w

FIG. 6

FIG. 7

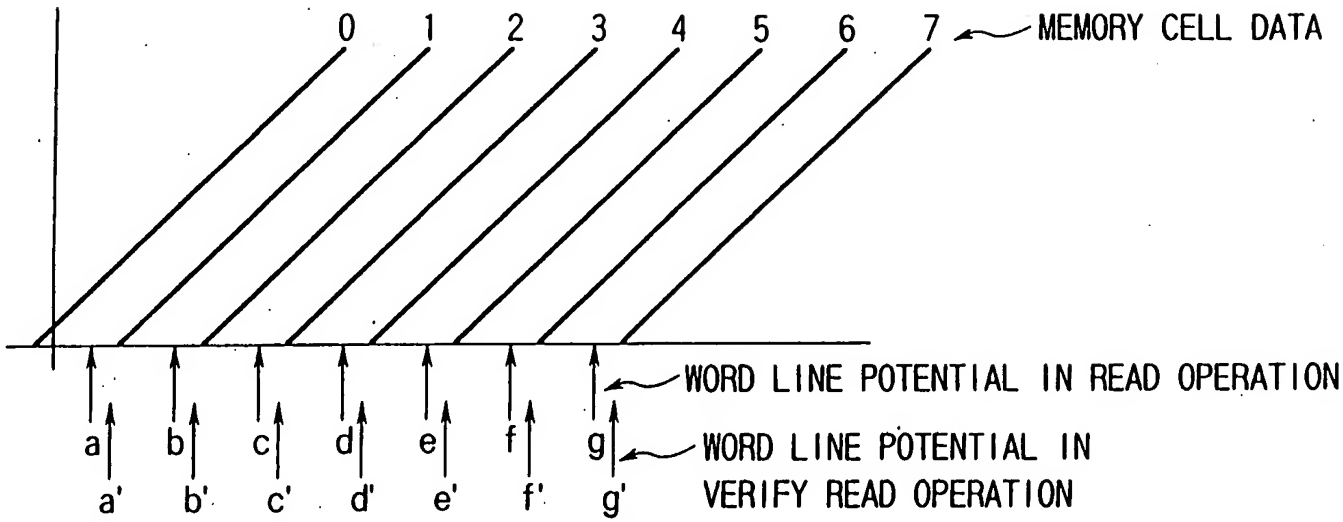


FIG. 8

MEMORY CELL DATA	MEMORY CELL THRESHOLD VALUE	DATA TO BE WRITTEN AND READ		
		1st PAGE	2nd PAGE	3rd PAGE
0	NOT HIGHER THAN 0V	1	1	1
1	0.3V~0.5V	1	1	0
2	0.8V~1.0V	1	0	1
3	1.3V~1.5V	1	0	0
4	1.8V~2.0V	0	1	1
5	2.3V~2.5V	0	1	0
6	2.8V~3.0V	0	0	1
7	3.3V~3.5V	0	0	0

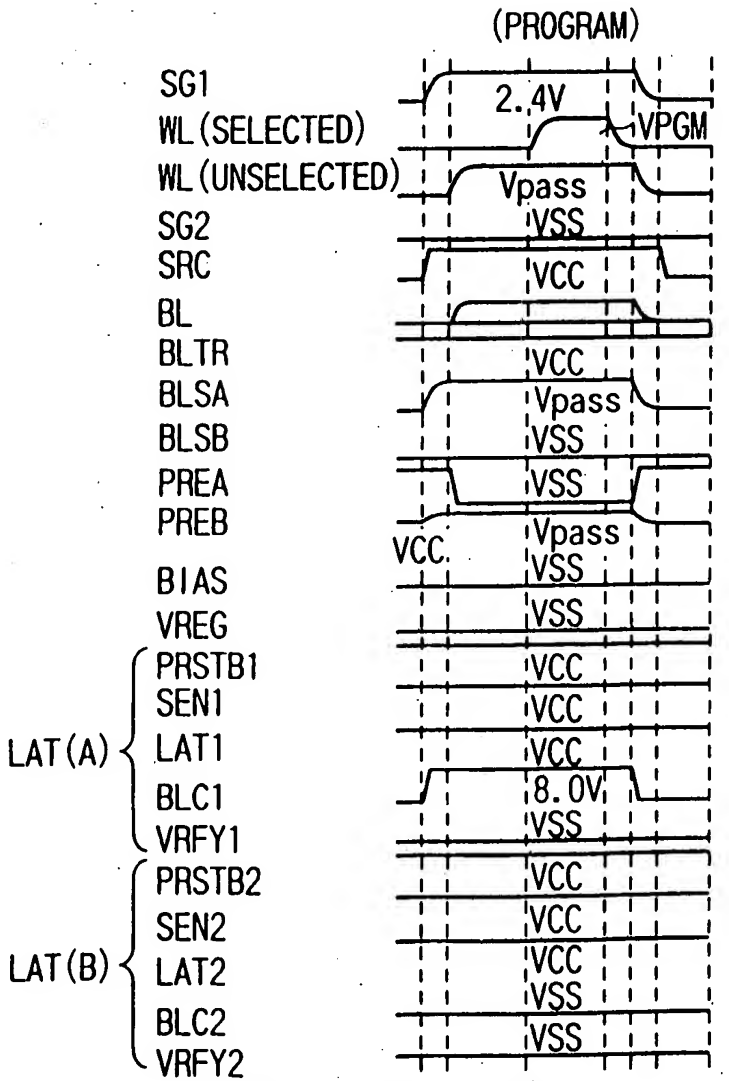


FIG. 9

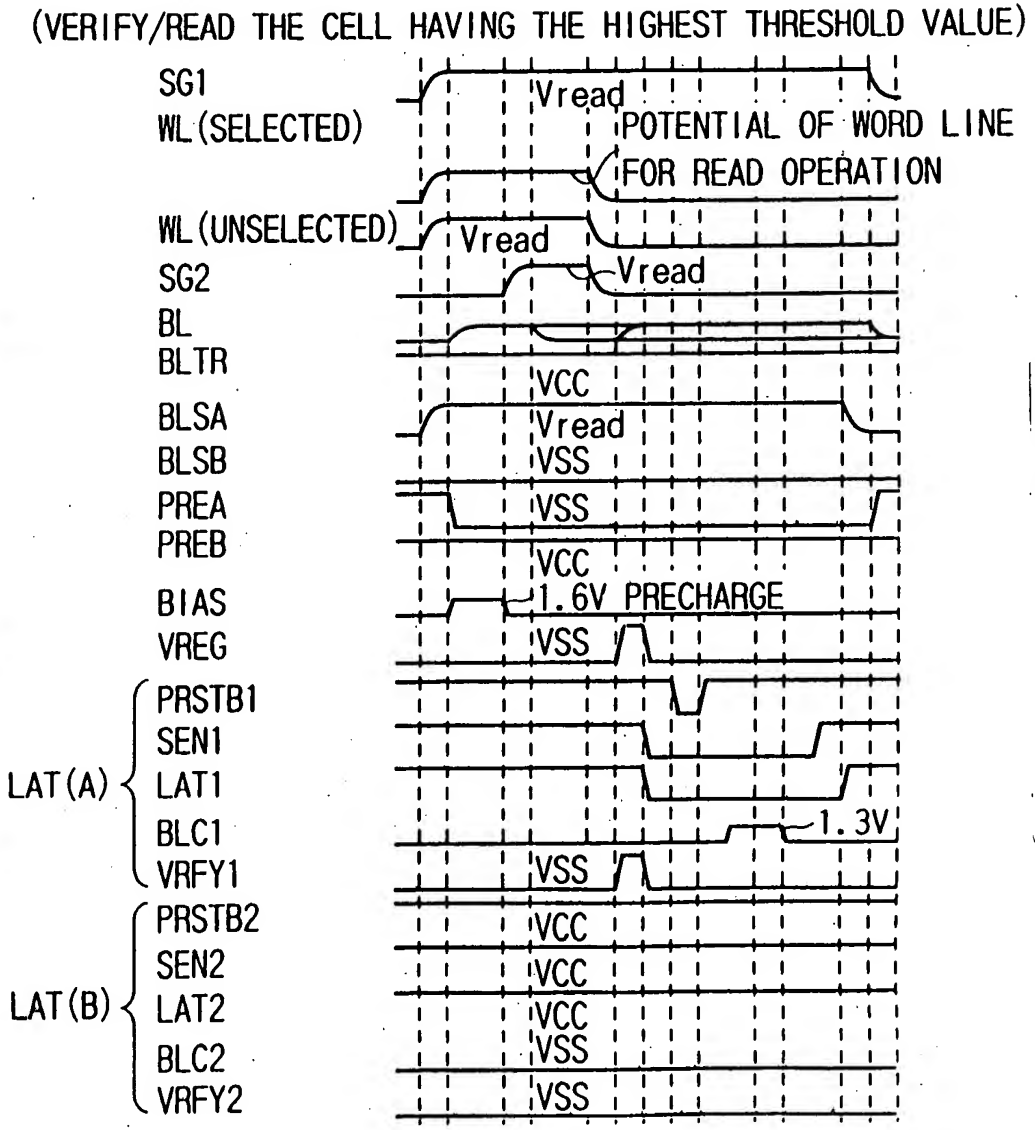


FIG. 10

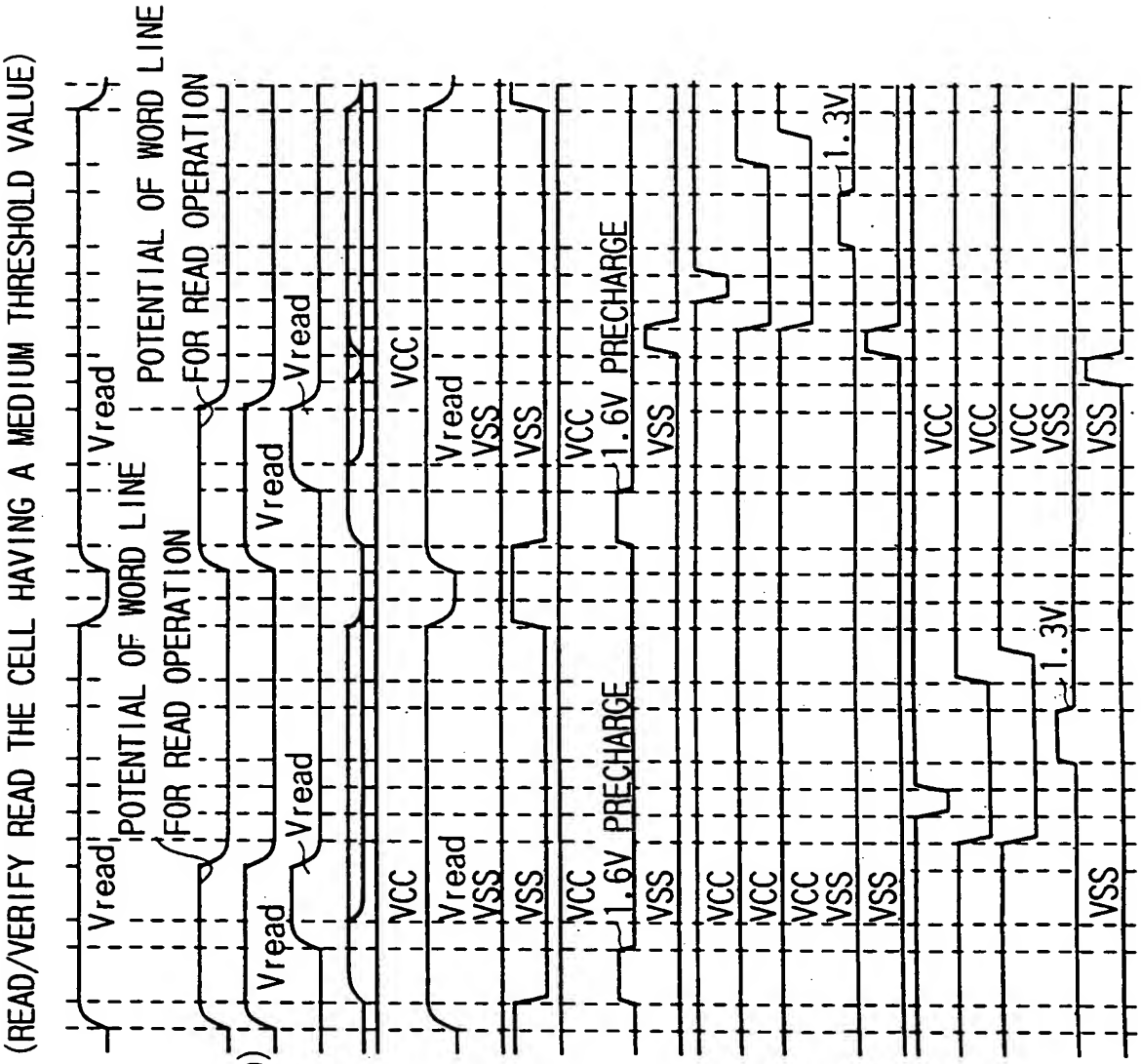

(READ/VERIFY READ THE CELL HAVING A MEDIUM THRESHOLD VALUE)
SG1
WL (SELECTED)
WL (UNSELECTED)
SG2
BL
BLTR
BLSA
BLSB
PREA
PREB
BIAS
VREG
PRSTB1
SEN1
LAT1
BLC1
VRFY1
PRSTB2
SEN2
LAT2
BLC2
VRFY2
LAT(A)
LAT(B)
Vread
POTENTIAL OF WORD LINE FOR READ OPERATION
VCC
VSS
1.6V PRECHARGE
1.3V

FIG. 11

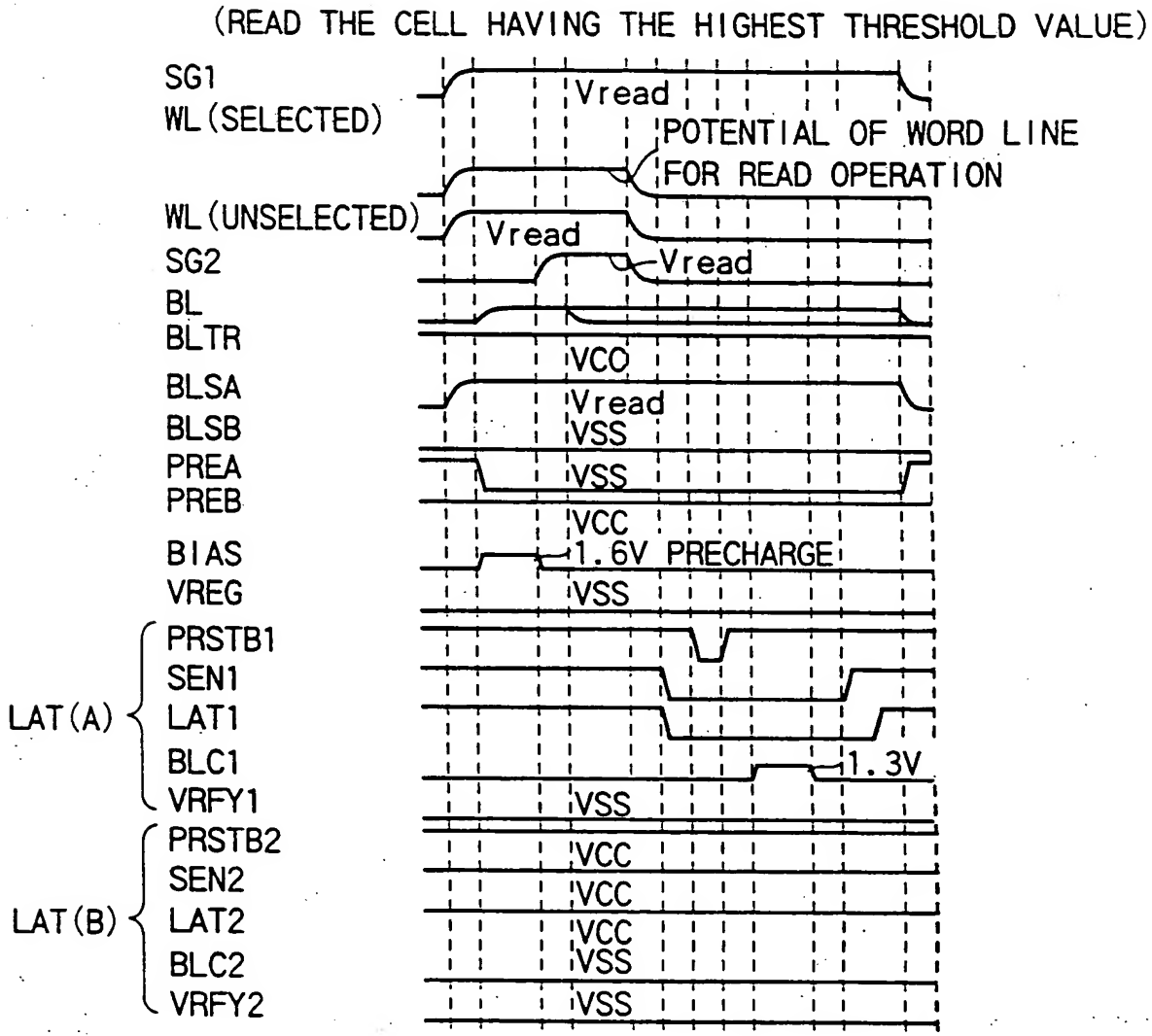

(READ THE CELL HAVING THE HIGHEST THRESHOLD VALUE)
SG1
WL(SELECTED)
WL(UNSELECTED)
SG2
BL
BLTR
BLSA
BLSB
PREA
PREB
BIAS
VREG
LAT(A)
PRSTB1
SEN1
LAT1
BLC1
VRFY1
LAT(B)
PRSTB2
SEN2
LAT2
BLC2
VRFY2
Vread
POTENTIAL OF WORD LINE
FOR READ OPERATION
Vread
Vread
VCO
Vread
VSS
VSS
VCC
1.6V PRECHARGE
VSS
1.3V
VSS
VCC
VCC
VCC
VSS
VSS

FIG. 12

PROG. VERIFY (1st PAGE)

0	0→4		MEMORY CELL DATA	
INHIBIT A B BIT	WRITE(OK) A B BIT	WRITE(NG) A B BIT	A=LAT(A), B=LAT(B), BIT=BL	
H	L	L	DATA LOADING (WRITE→L, INHIBIT→H FOR A)	
H L H H H H	L H L H H H	L L L L L L	READ AT d' BIT LINE IS AT H WHEN A IS H (VRFY1) POTENTIAL OF BIT LINE IS APPLIED TO A	0→4 VERIFY

FIG. 13A

PROG. VERIFY (2nd PAGE)

0	0→2		4	4→6		MEMORY CELL DATA	
INHIBIT A B BIT	WRITE(OK) A B BIT	WRITE(NG) A B BIT	INHIBIT A B BIT	WRITE(OK) A B BIT	WRITE(NG) A B BIT	A=LAT(A), B=LAT(B), BIT=BL	
H	L		H	L	L	DATA LOADING (WRITE→L, INHIBIT→H FOR A)	
H L H H H H	L L L L L L		H L H H H H	L H L H H H	L L L L L L	READ AT f' BIT LINE IS AT H WHEN A IS H (VRFY1) POTENTIAL OF BIT LINE IS APPLIED TO A	4→6 VERIFY

FIG. 13B

PROG. VERIFY (2nd PAGE)

H	L	L	H	L		DATA LOADING	
H L H L L	L L L L L	L L L L L	H H H H H	L H L H H		READ AT d' POTENTIAL OF BIT LINE IS APPLIED TO B (FIRST TIME OF LOOP)	10→2 VERIFY
H L L H L L H L H H L H	L L H L L H L L H H L H	L L L L L L L L L L L L	H H H H H L H H H H H H	L H H L H L L H L L H L		READ AT b' BIT LINE IS AT L WHEN B IS H (VRFY2) BIT LINE IS AT H WHEN A IS H (VRFY1) POTENTIAL OF BIT LINE IS APPLIED TO A	

FIG. 13C

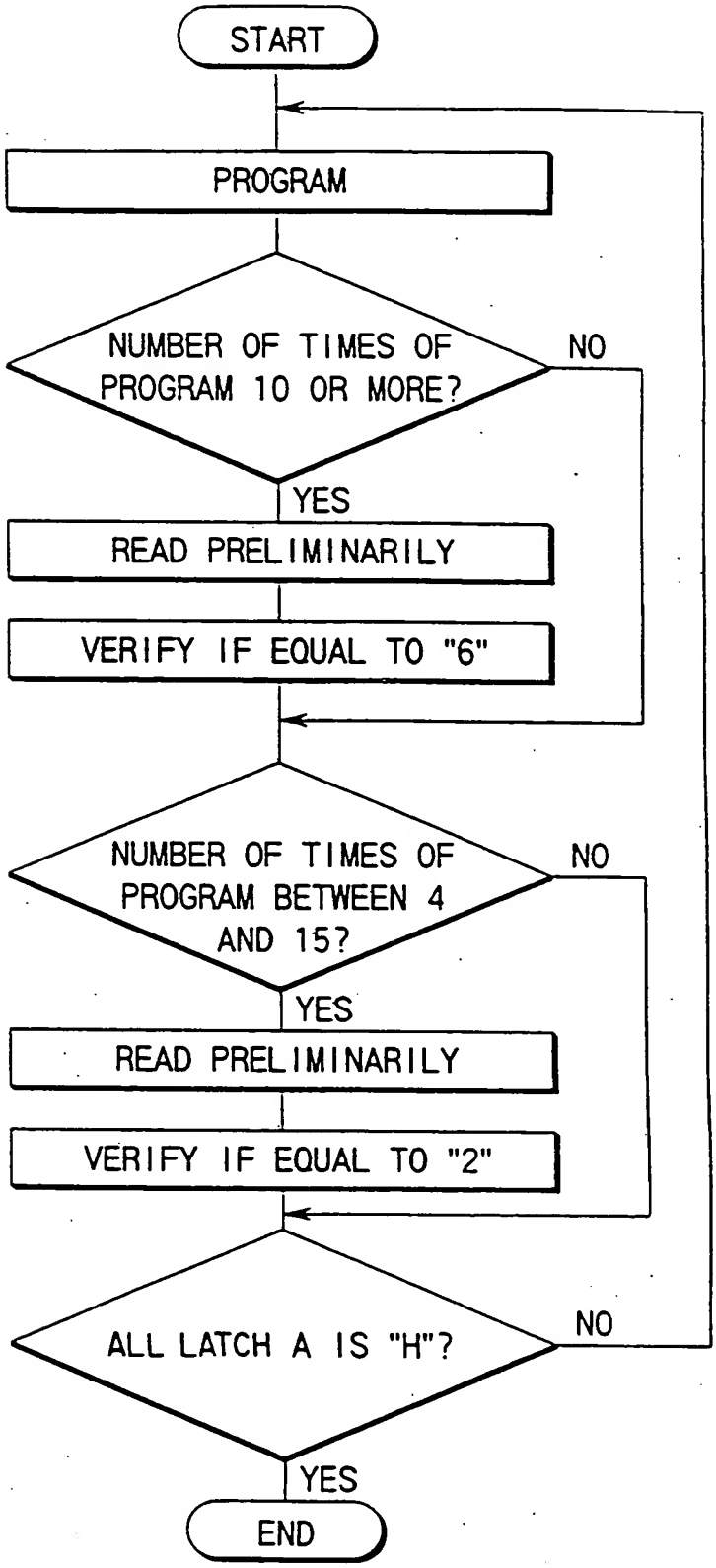

START
PROGRAM
NUMBER OF TIMES OF PROGRAM 10 OR MORE?
NO
YES
READ PRELIMINARILY
VERIFY IF EQUAL TO "6"
NUMBER OF TIMES OF PROGRAM BETWEEN 4 AND 15?
NO
YES
READ PRELIMINARILY
VERIFY IF EQUAL TO "2"
ALL LATCH A IS "H"?
NO
YES
END

FIG. 13D

PROG. VERIFY (3rd PAGE)

0	0→1		2	2→3		4	4→5	
INHIBIT A B BIT	WRITE(OK) A B BIT	WRITE(NG) A B BIT	INHIBIT A B BIT	WRITE(OK) A B BIT	WRITE(NG) A B BIT	INHIBIT A B BIT	WRITE(OK) A B BIT	WRITE(NG) A B BIT
H	L		H	L		H	L	
H L H H H H	L L L L L L		H L H H H H	L L L L L L		H L H H H H	L L L L L L	

FIG. 14A

6	6→7		MEMORY CELL DATA	
INHIBIT A B BIT	WRITE(OK) A B BIT	WRITE(NG) A B BIT	A=LAT(A), B=LAT(B), BIT=BL	
H	L	L	DATA LOADING (WRITE→L, INHIBIT→H FOR A)	
H L H H H H	L H L H H H	L L L L L L	READ AT g' BIT LINE IS AT H WHEN A IS H (VRFY1) POTENTIAL OF BIT LINE IS APPLIED TO A	6→7 VERIFY

FIG. 14B

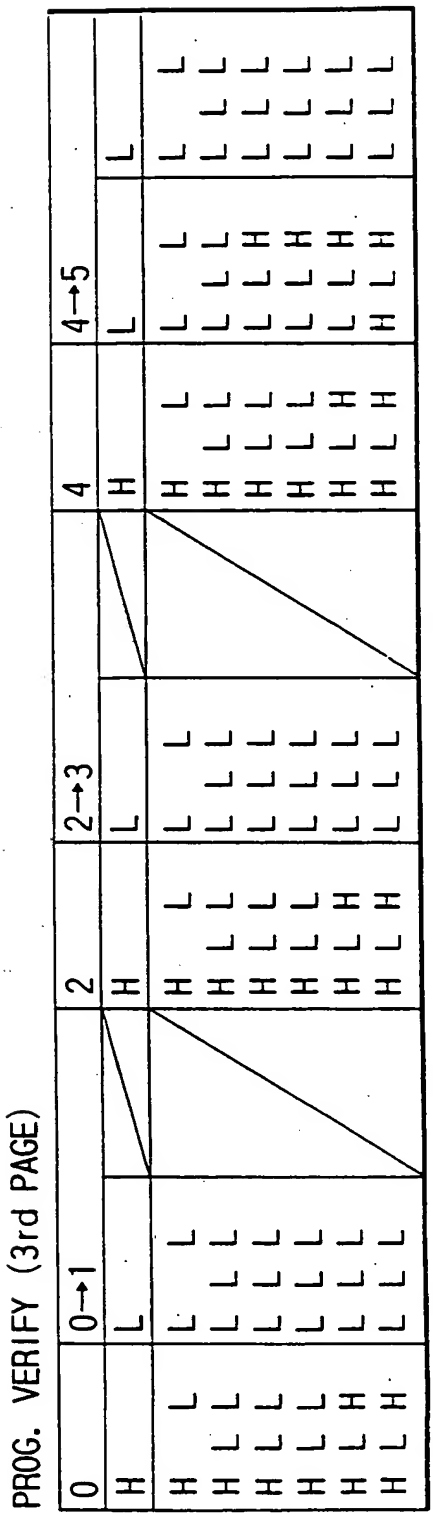


FIG. 15A

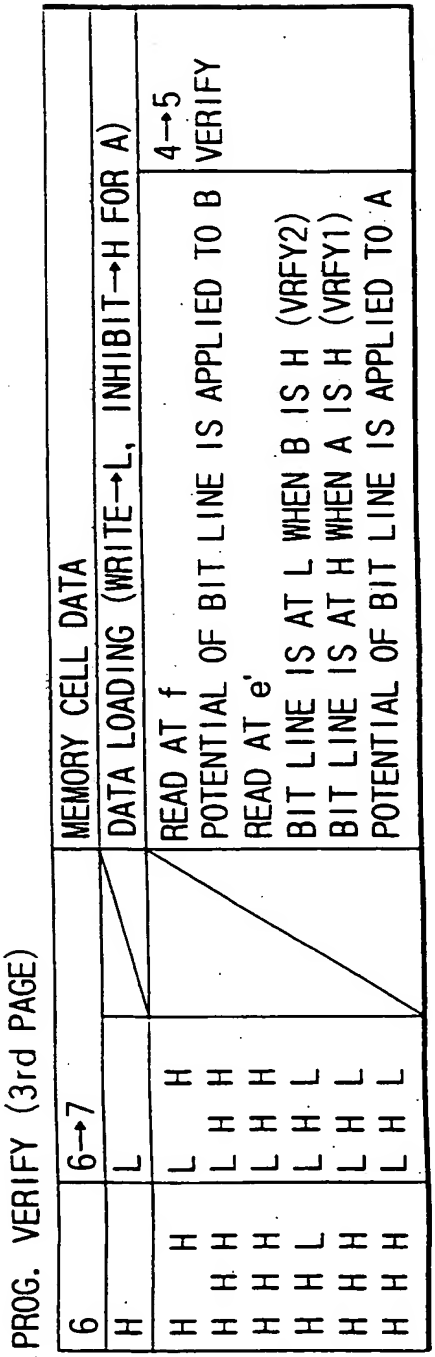


FIG. 15B

PROG. VERIFY (3rd PAGE)

0	0→1		2	2→3		4	4→5	
H	L		H	L	L	H	L	
H L	L L		H L	L L	L L	H H	L H	
H L	L L		H L	L L	L L	H H	L H	
H L	L L		H L	L L	L L	H H	L H	
H L	L L		H L	L L	L L	H H	L H	
H L	L L		H L	L L	L L	H H	L H	

FIG. 16A

PROG. VERIFY (3rd PAGE)

6	6→7		MEMORY CELL DATA	
H	L		DATA LOADING	
H H	L H		READ AT d	2→3
H H	L H		POTENTIAL OF BIT LINE IS APPLIED TO B	VERIFY
H H	L H		READ AT c'	
H L	L H		BIT LINE IS AT L WHEN B IS H (VRFY2)	
H H	L H		BIT LINE IS AT H WHEN A IS H (VRFY1)	
H H	L H		POTENTIAL OF BIT LINE IS APPLIED TO A	

FIG. 16B

A=LAT(A), B=LAT(B)

PROG. VERIFY (3rd PAGE)

0	0→1		2	2→3		4	4→5	
H	L	L	H	L		H	L	
H L	L L	L L	H H	L H		H H	L H	
H L L	L L H	L L L	H H H	L H H		H H H	L H H	
H L L	L L H	L L L	H H L	L H L		H H L	L H L	
H L H	L L H	L L L	H H H	L H L		H H H	L H L	
H L H	H L H	L L L	H H H	L H L		H H H	L H L	

FIG. 17A

PROG. VERIFY (3rd PAGE)

6	6→7		MEMORY CELL DATA	
H	L		DATA LOADING	
H H	L H		READ AT b POTENTIAL OF BIT LINE IS APPLIED TO B READ AT a' BIT LINE IS AT L WHEN B IS H (VRFY2) BIT LINE IS AT H WHEN A IS H (VRFY1) POTENTIAL OF BIT LINE IS APPLIED TO A	0→1 VERIFY
H H H	L H H			
H H H	L H H			
H H L	L H L			
H H H	L H L			
H H H	L H L			

FIG. 17B

A=LAT(A), B=LAT(B)

READ (1st PAGE)

0,1,2,3	4,5,6,7		
A B BIT	A B BIT	A=LAT(A), B=LAT(B), BIT=BL	
L	H	READ AT d	01234567
L L	H H	POTENTIAL OF BITI LINE IS APPLIED TO A	READ

FIG. 18A

READ (2nd PAGE)

0,1	2,3	4,5	6,7		
A B BIT	A B BIT	A B BIT	A B BIT	A=LAT(A), B=LAT(B), BIT=BL	
L	L	L	H	READ AT f	45,67 READ
L L	L L	L L	H H	POTENTIAL OF BITI LINE IS APPLIED TO A	

FIG. 18B

READ (2nd PAGE)

L L	L L	L H	H H	READ AT d	01,23 READ
L L L	L L L	L H H	H H H	POTENTIAL OF BIT LINE IS APPLIED TO B	
L L L	L L H	L H H	H H H	READ AT b	
L L L	L L H	L H L	H H L	BIT LINE IS AT L WHEN B IS H (VRFY2)	
L L L	L L H	L H L	H H H	BIT LINE IS AT H WHEN A IS H (VRFY1)	
L L L	H L H	L H L	H H H	POTENTIAL OF BIT LINE IS APPLIED TO A	

FIG. 18C

READ (3rd PAGE)

0			1			2			3			4			5			6			7			A=LAT(A), B=LAT(B), BIT=BL	
A	B	BIT	A	B	BIT	A	B	BIT	A	B	BIT	A	B	BIT	A	B	BIT	A	B	BIT	A	B	BIT		
		L			L			L			L			L			L			L			H	READ AT g	67
L		L	L		L	L		L	L		L	L		L	L		L	L		L	H		H	POTENTIAL OF BITI LINE IS APPLIED TO A	READ

FIG. 19A

READ (3rd PAGE)

L		L	L		L	L		L	L		L	L		L	L		H	H		H	READ AT f	4,5 READ
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	POTENTIAL OF BIT LINE IS APPLIED TO B	
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	H	H	H	H	READ AT e	
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	H	H	L	BIT LINE IS AT L WHEN B IS H (VRFY2)	
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	H	H	H	BIT LINE IS AT H WHEN A IS H (VRFY1)	
L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	H	L	H	H	H	POTENTIAL OF BIT LINE IS APPLIED TO A.	

FIG. 19B

READ (3rd PAGE)

L		L	L		L	L		L	L		L	L		H	H		H	L		H	H		H	READ AT d	2,3 READ
L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	POTENTIAL OF BIT LINE IS APPLIED TO B	
L	L	L	L	L	L	L	L	L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	READ AT c	
L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	H	H	L	L	H	L	H	H	L	BIT LINE IS AT L WHEN B IS H (VRFY2)	
L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	H	H	H	L	H	L	H	H	H	BIT LINE IS AT H WHEN A IS H (VRFY1)	
L	L	L	L	L	L	L	L	L	H	L	H	L	H	L	H	H	H	L	H	L	H	H	H	POTENTIAL OF BIT LINE IS APPLIED TO A	

FIG. 19C

READ (3rd PAGE)

L		L	L		L	L		H	H		H	L		H	H		H	L		H	H		H	READ AT b	0,1 READ
L	L	L	L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	L	H	H	H	H	H	POTENTIAL OF BIT LINE IS APPLIED TO B	
L	L	L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	L	H	H	H	H	H	READ AT a	
L	L	L	L	L	H	L	H	L	H	H	L	L	H	L	H	H	L	L	H	L	H	H	L	BIT LINE IS AT L WHEN B IS H (VRFY2)	
L	L	L	L	L	H	L	H	L	H	H	H	L	H	L	H	H	H	L	H	L	H	H	H	BIT LINE IS AT H WHEN A IS H (VRFY1)	
L	L	L	H	L	H	L	H	L	H	H	H	L	H	L	H	H	H	L	H	L	H	H	H	POTENTIAL OF BIT LINE IS APPLIED TO A	

FIG. 19D

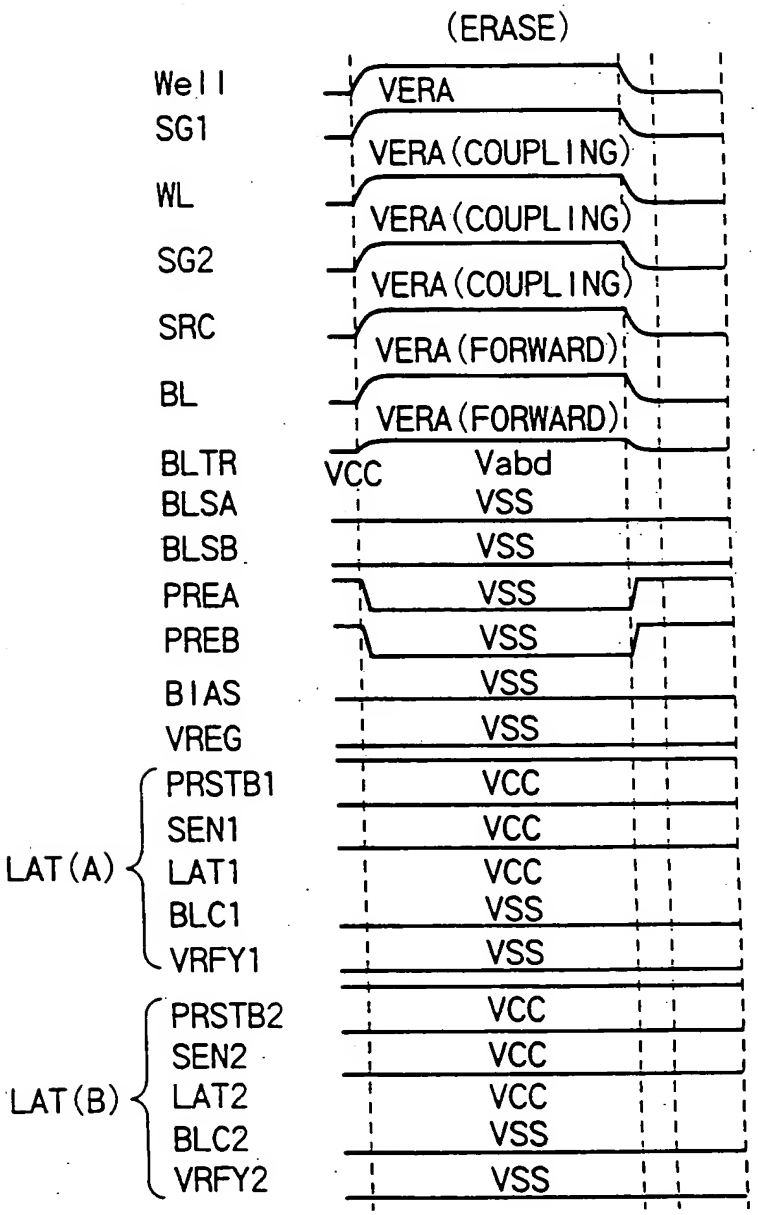

(ERASE)
Well
SG1
WL
SG2
SRC
BL
BLTR
BLSA
BLSB
PREA
PREB
BIAS
VREG
LAT(A)
PRSTB1
SEN1
LAT1
BLC1
VRFY1
LAT(B)
PRSTB2
SEN2
LAT2
BLC2
VRFY2
VERA
VERA(COUPLING)
VERA(COUPLING)
VERA(COUPLING)
VERA(FORWARD)
VERA(FORWARD)
VCC
Vabd
VSS
VSS
VSS
VSS
VSS
VCC
VCC
VCC
VSS
VSS
VCC
VCC
VCC
VSS
VSS

FIG. 20

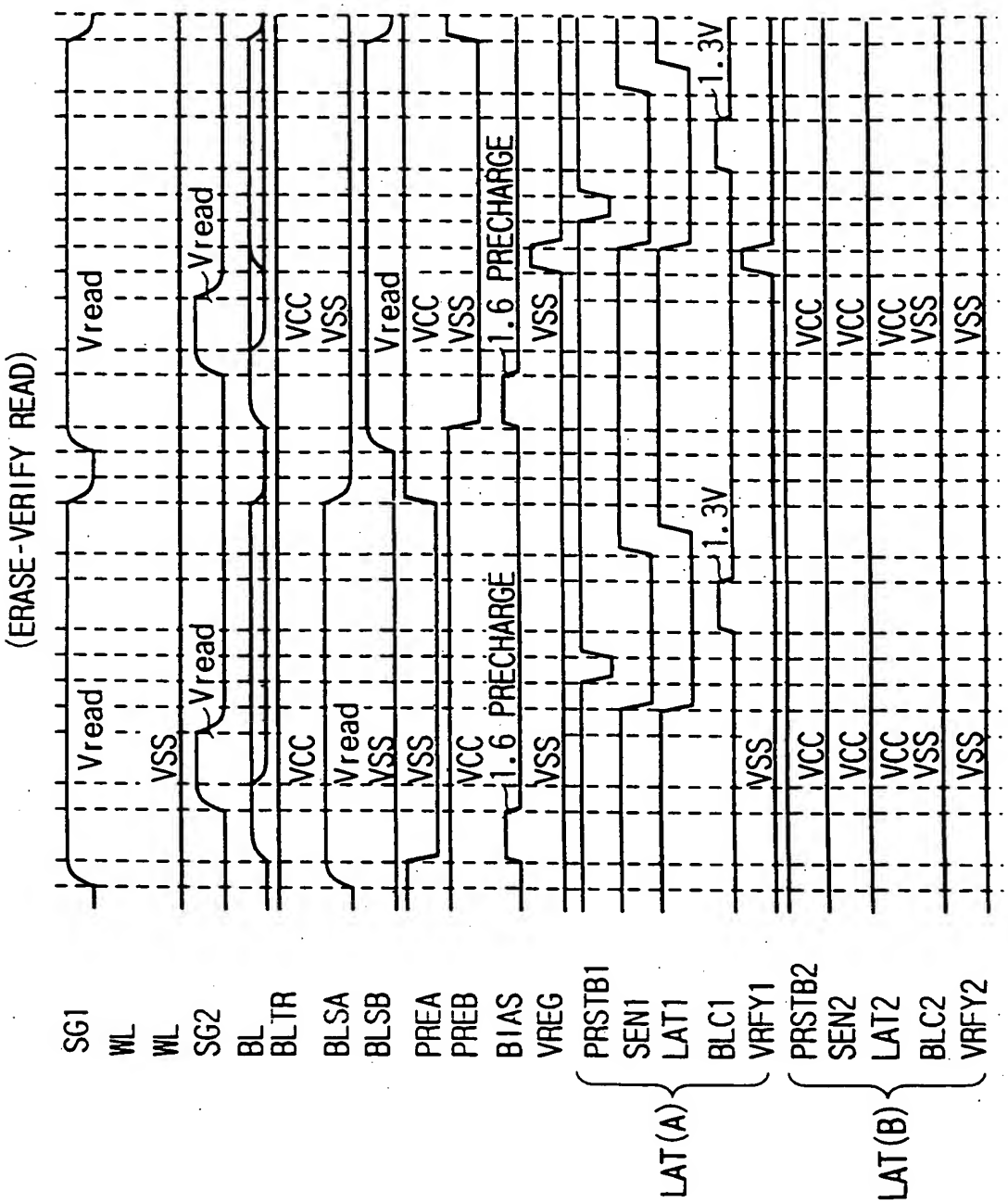

(ERASE-VERIFY READ)
SG1
WL
WL
SG2
BL
BLTR
BLSA
BLSB
PREA
PREB
BIAS
VREG
PRSTB1
SEN1
LAT1
BLC1
VRFY1
PRSTB2
SEN2
LAT2
BLC2
VRFY2
LAT(A)
LAT(B)
Vread
VSS
VCC
1.6 PRECHARGE
1.3V

FIG. 21

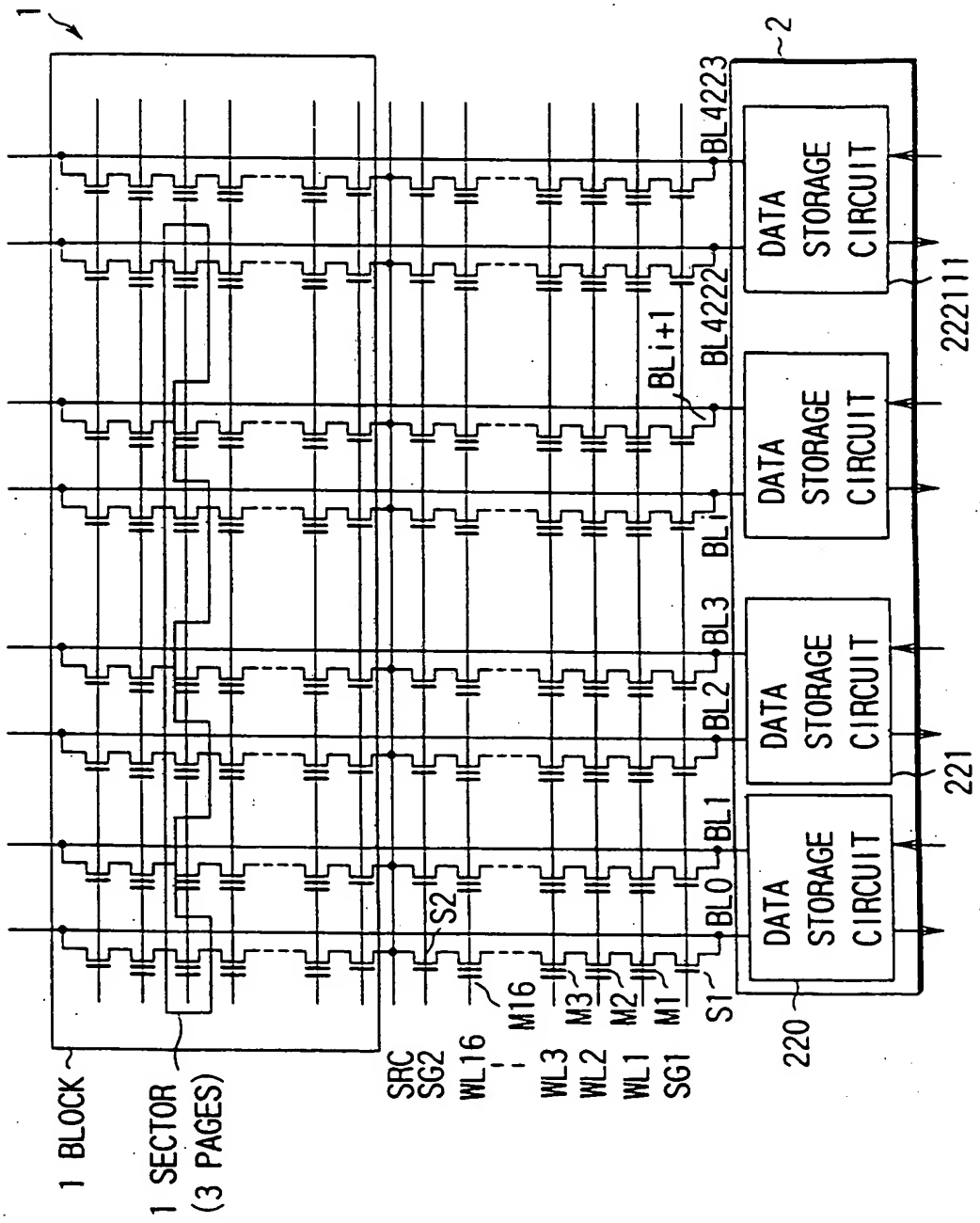

1
2
1 BLOCK
1 SECTOR
(3 PAGES)
SRC
SG2
WL16
WL3
WL2
WL1
SG1
S2
M16
M3
M2
M1
S1
BL0
BL1
BL2
BL3
BLi+1
BL4222
BL4223
220
221
222111
DATA STORAGE CIRCUIT
DATA STORAGE CIRCUIT
DATA STORAGE CIRCUIT
DATA STORAGE CIRCUIT

FIG. 22

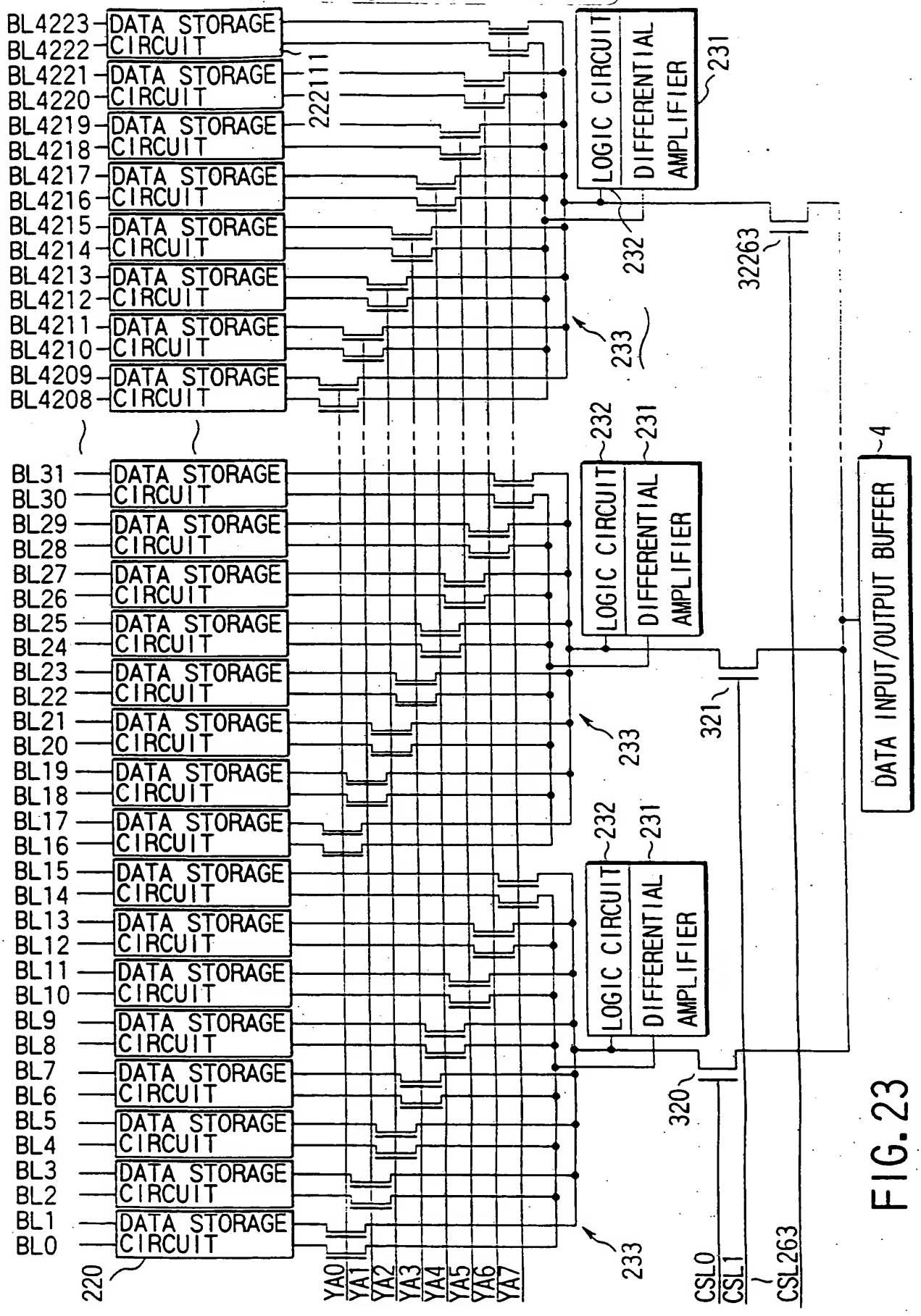

BL4223
BL4222
BL4221
BL4220
BL4219
BL4218
BL4217
BL4216
BL4215
BL4214
BL4213
BL4212
BL4211
BL4210
BL4209
BL4208
DATA STORAGE CIRCUIT
222111
LOGIC CIRCUIT
DIFFERENTIAL AMPLIFIER
231
232
233
32263
BL31
BL30
BL29
BL28
BL27
BL26
BL25
BL24
BL23
BL22
BL21
BL20
BL19
BL18
BL17
BL16
BL15
BL14
BL13
BL12
BL11
BL10
BL9
BL8
BL7
BL6
BL5
BL4
BL3
BL2
BL1
BL0
321
320
4
DATA INPUT/OUTPUT BUFFER
220
YA0
YA1
YA2
YA3
YA4
YA5
YA6
YA7
CSL0
CSL1
CSL263

FIG. 23

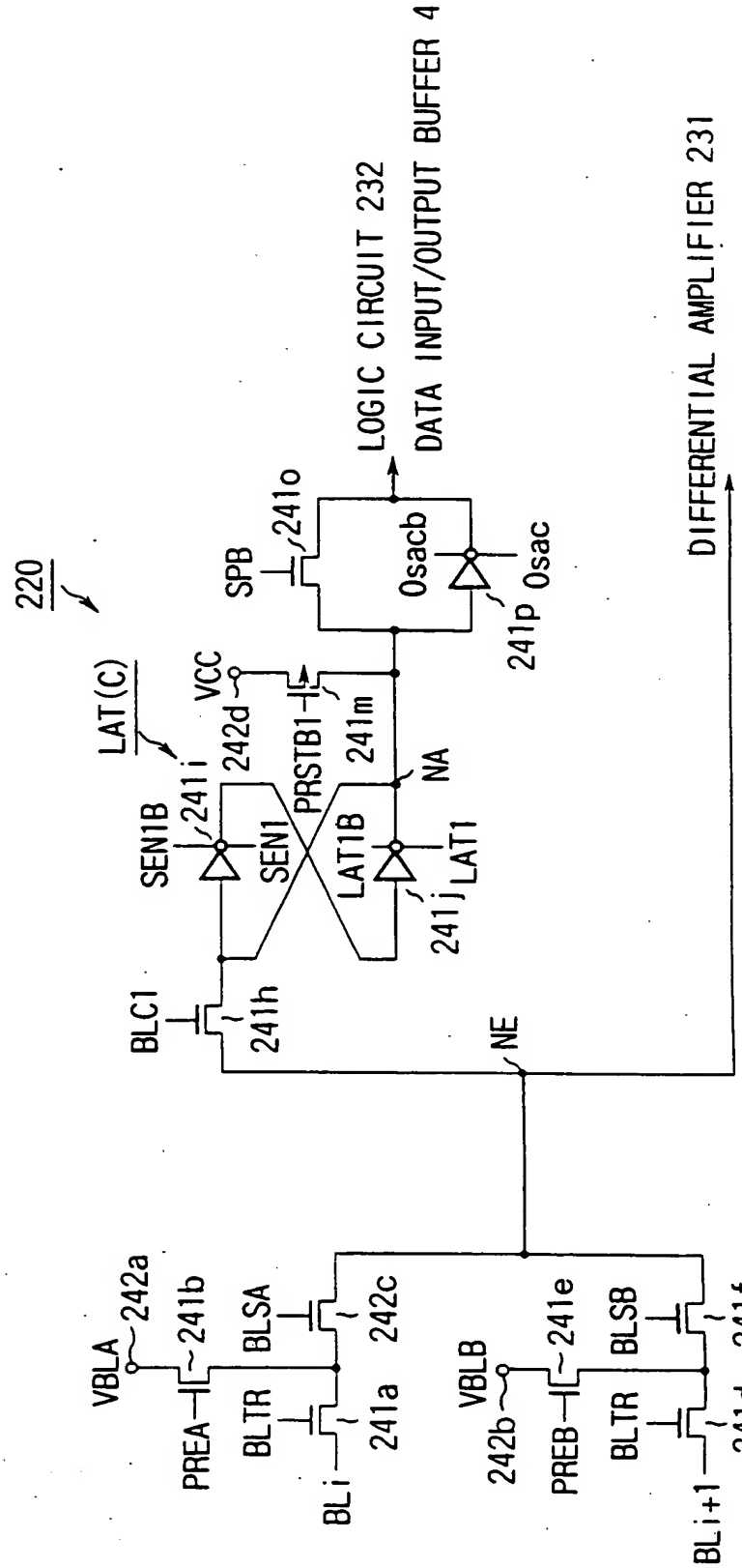

220
LOGIC CIRCUIT 232
DATA INPUT/OUTPUT BUFFER 4
DIFFERENTIAL AMPLIFIER 231
SPB
241o
Osacb
Osac
241p
LAT(C)
241i
SEN1B
SEN1
PRSTB1
241m
242d
VCC
NA
LAT1B
LAT1
241j
BLC1
241h
NE
VBLA
242a
241b
PREA
BLTR
BLi
241a
BLSA
242c
VBLB
242b
PREB
241e
BLTR
BLi+1
241d
BLSB
241f

FIG. 24

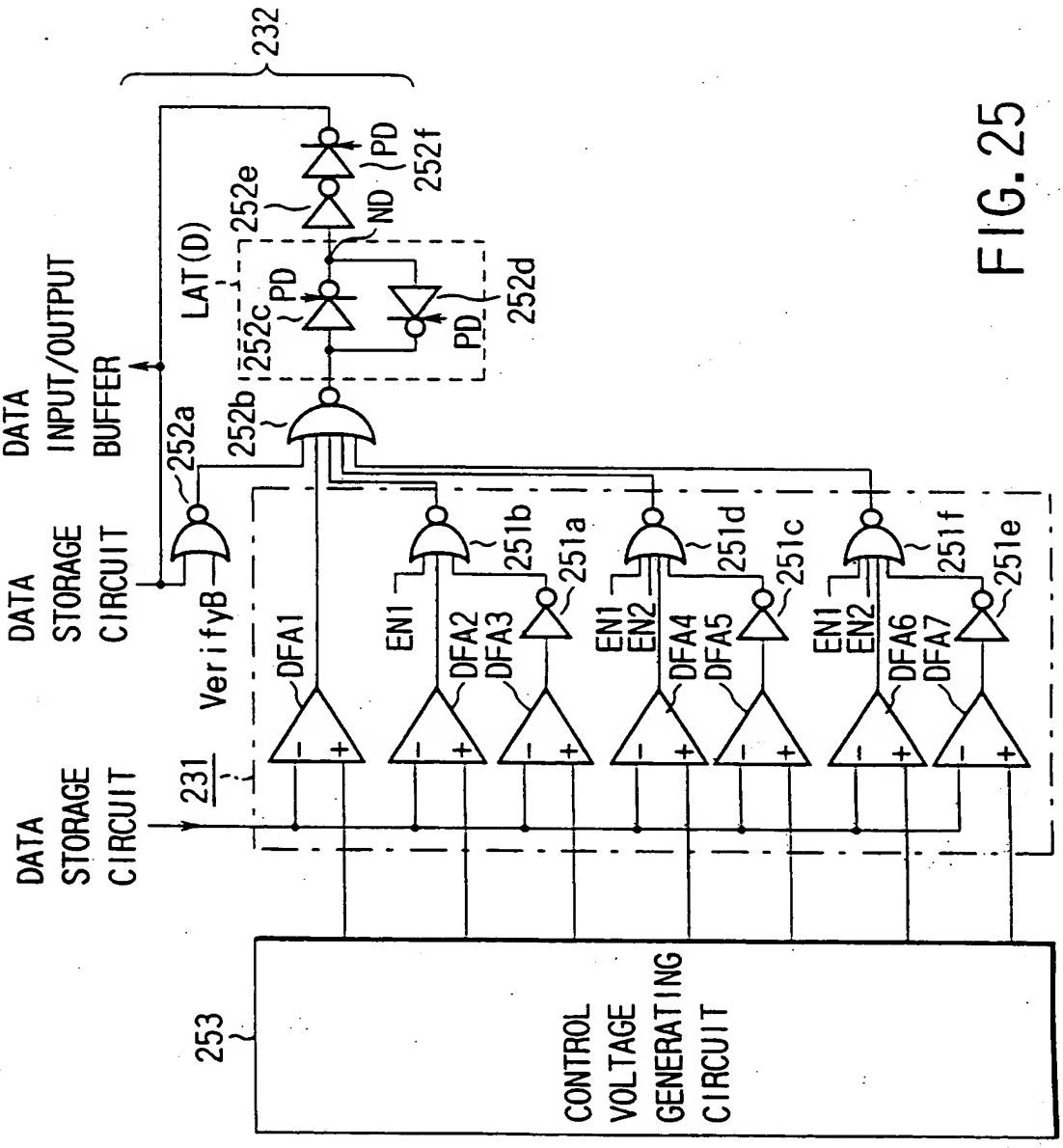

232
DATA INPUT/OUTPUT BUFFER
LAT(D)
252a
252b
252c
252d
252e
252f
PD
ND
DATA STORAGE CIRCUIT
VerifyB
DFA1
EN1
DFA2
DFA3
EN1
EN2
DFA4
DFA5
EN1
EN2
DFA6
DFA7
251a
251b
251c
251d
251e
251f
231
DATA STORAGE CIRCUIT
253
CONTROL VOLTAGE GENERATING CIRCUIT

FIG. 25

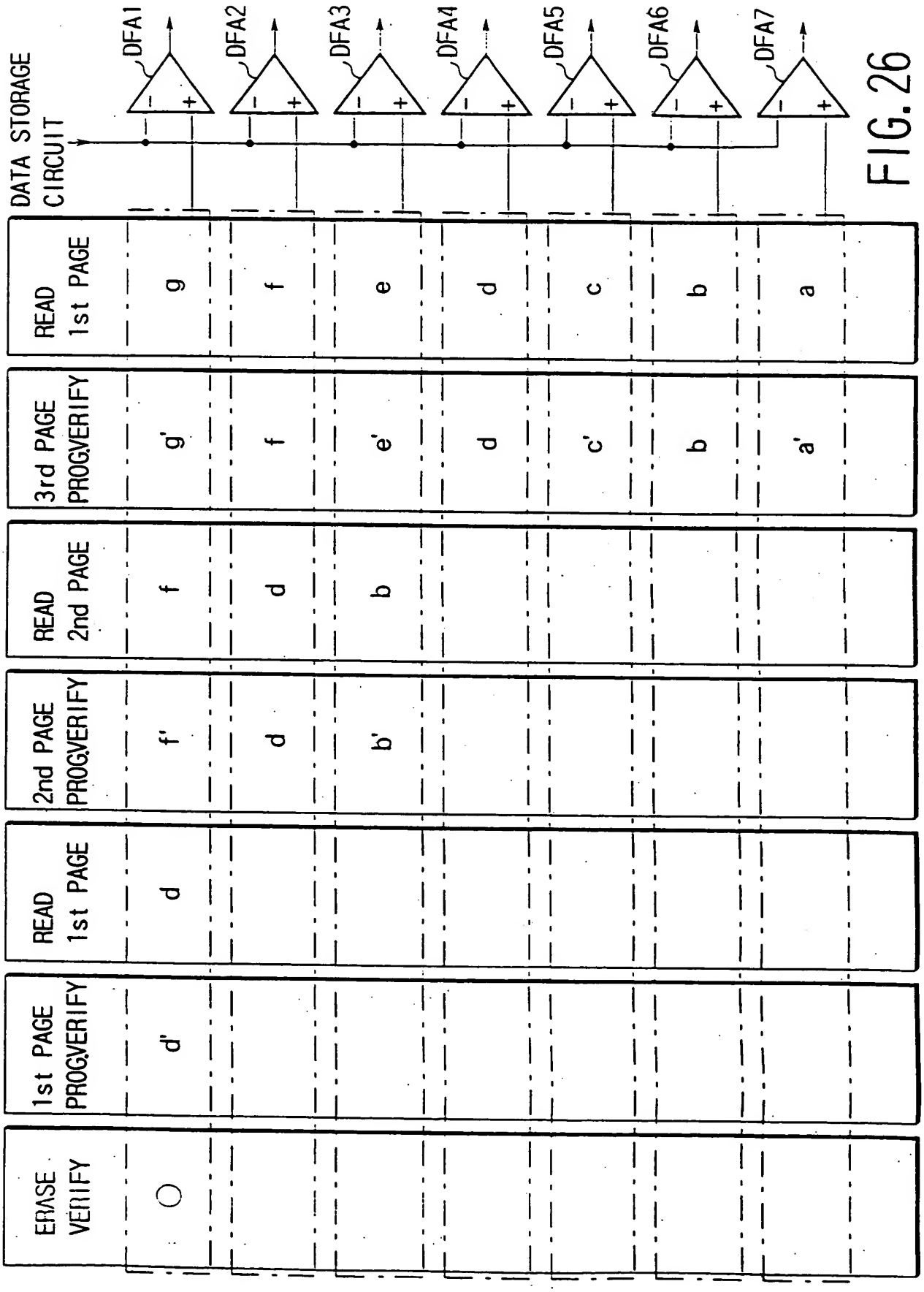

DATA STORAGE CIRCUIT
DFA1
DFA2
DFA3
DFA4
DFA5
DFA6
DFA7
ERASE VERIFY
1st PAGE PROGVERIFY
READ 1st PAGE
2nd PAGE PROGVERIFY
READ 2nd PAGE
3rd PAGE PROGVERIFY
READ 1st PAGE
d'
d
f'
d
b'
f
d
b
g'
f
e'
d
c'
b
a'
g
f
e
d
c
b
a

FIG. 26

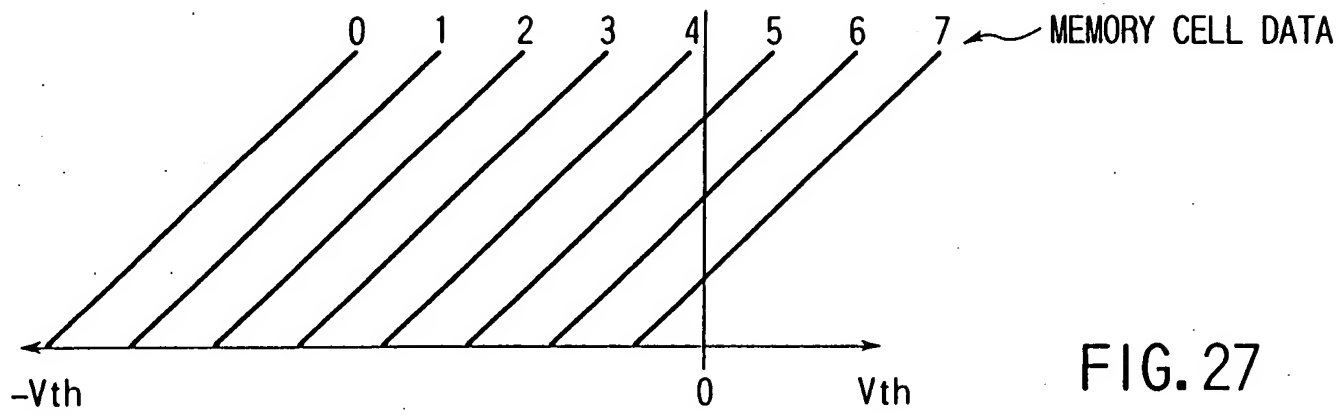
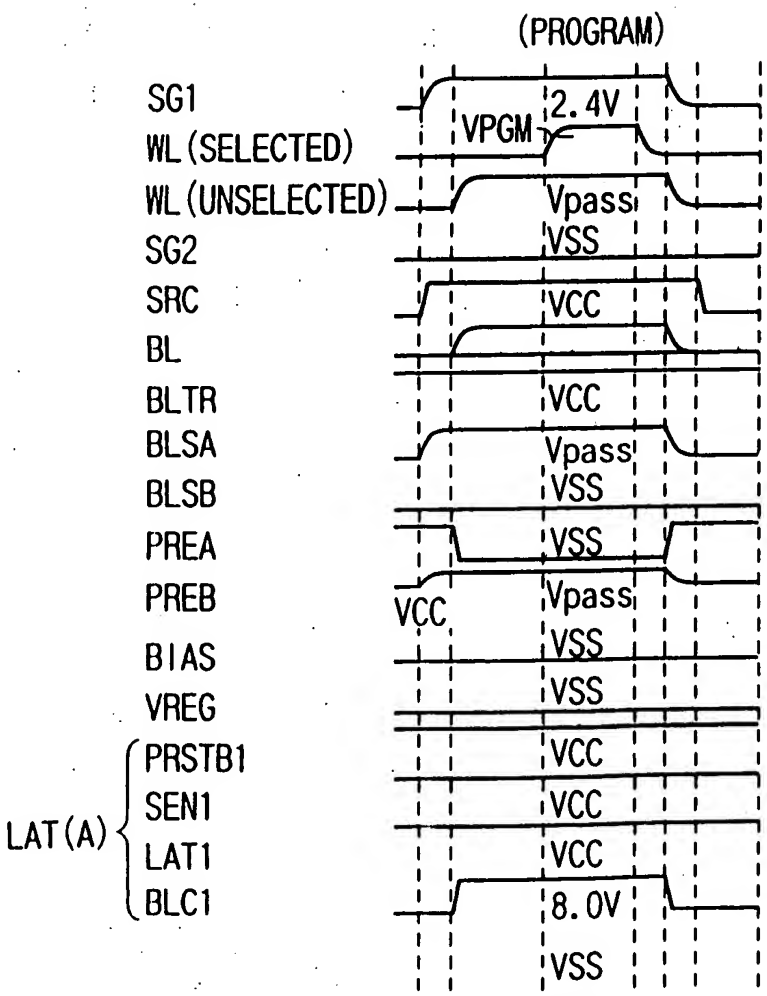


FIG. 27

MEMORY CELL DATA	MEMORY CELL THRESHOLD VALUE	VOLTAGE READ OUT TO BIT LINE	DATA TO BE WRITTEN AND READ		
			1st PAGE	2nd PAGE	3rd PAGE
0	NOT HIGHER THAN -3.8V	3.8V~4.0V	1	1	1
1	-3.5V~-3.3V	3.3V~3.5V	1	1	0
2	-3.0V~-2.8V	2.8V~3.0V	1	0	1
3	-2.5V~-2.3V	2.3V~2.5V	1	0	0
4	-2.0V~-1.8V	1.8V~2.0V	0	1	1
5	-1.5V~-1.3V	1.3V~1.5V	0	1	0
6	-1.0V~-0.8V	0.8V~1.0V	0	0	1
7	-0.5V~-0.3V	0.3V~0.5V	0	0	0

FIG. 28



VCC:WHEN DATA IS EQUAL TO "1"
(NO WRITE OPERATION OCCURS)
VSS:WHEN DATA IS EQUAL TO "0"
(A WRITE OPERATION OCCURS)

FIG. 29

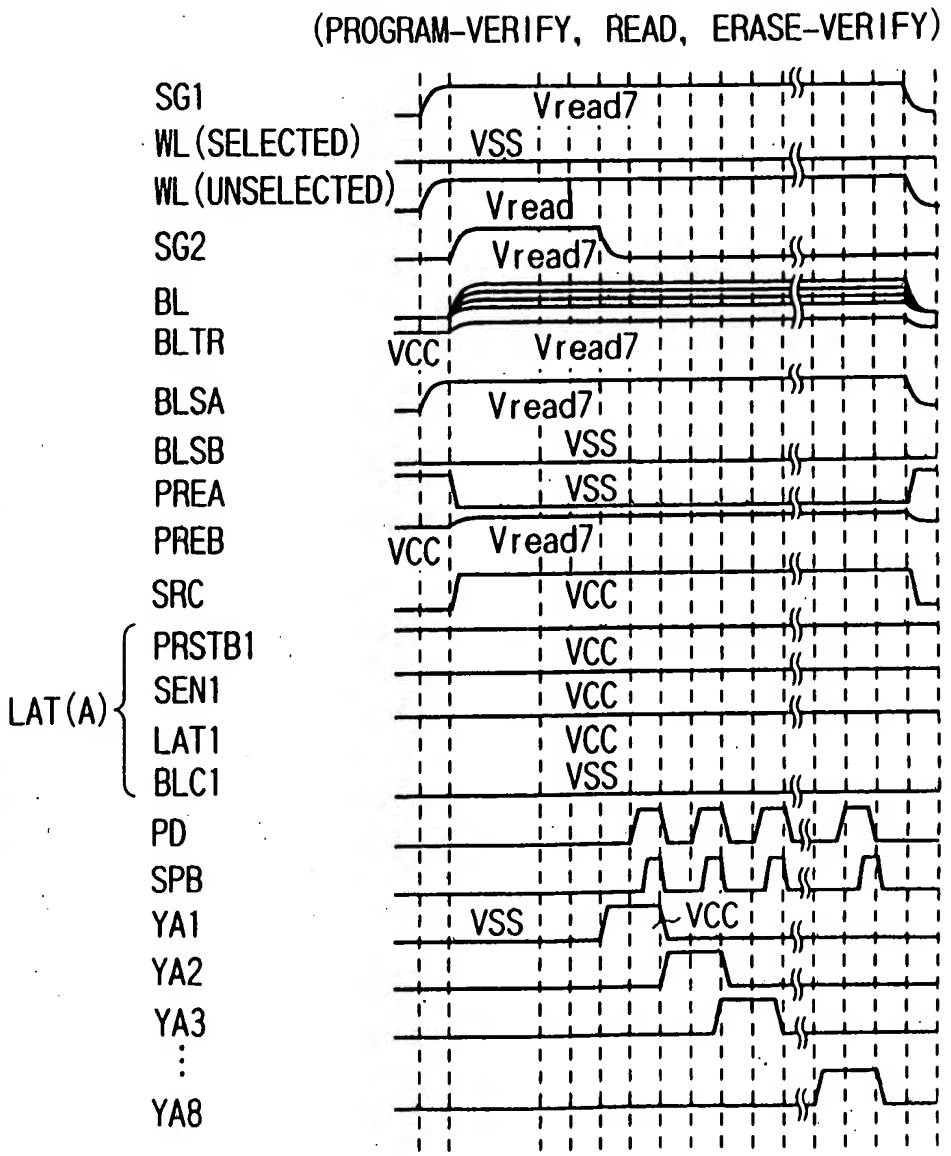


FIG. 30

REFERENCE POTENTIAL				
READ TIME		PROGRAM-VERIFY TIME		ERASE-VERIFY TIME
a	3.6V	a'	3.5V	○
b	3.1V	b'	3.0V	
c	2.6V	c'	2.5V	
d	2.1V	d'	2.0V	
e	1.6V	e'	1.5V	
f	1.1V	f'	1.0V	
g	0.6V	g'	0.5V	4.0V

FIG. 31

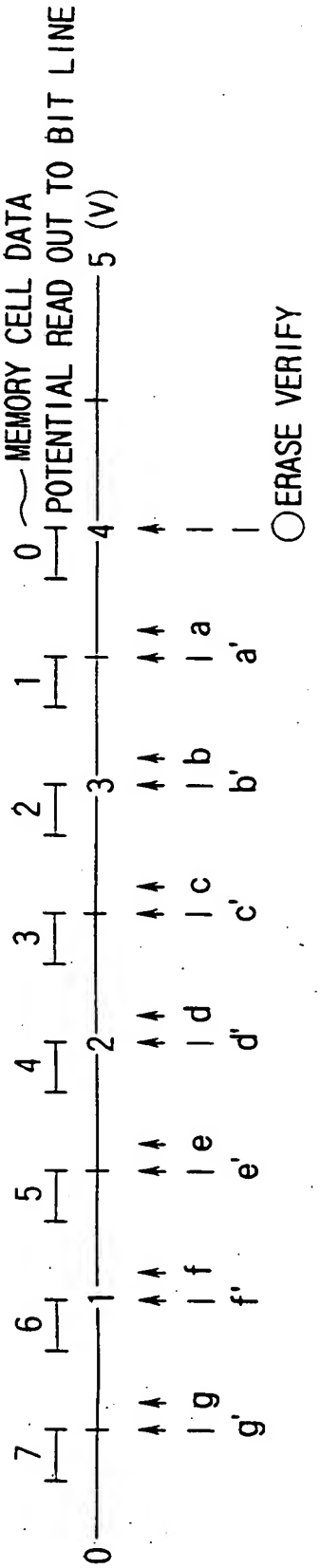


FIG. 32

VERIFY-1st PAGE		
POTENTIAL READ OUT TO BIT LINE	DFA1	LATCHED DATA
NOT HIGHER THAN d'	H	H
NOT LOWER THAN d'	L	L

FIG. 33A

VERIFY-2nd PAGE				
POTENTIAL READ OUT TO BIT LINE	DFA1	DFA2	DFA3	LATCHED DATA
NOT HIGHER THAN f'	H	H	H	H
NOT HIGHER THAN d AND NOT LOWER THAN f'	L	H	H	L
NOT HIGHER THAN b' AND NOT LOWER THAN d	L	L	H	H
NOT LOWER THAN b'	L	L	L	L

FIG. 33B

VERIFY-3rd PAGE								
POTENTIAL READ OUT TO BIT LINE	DFA1	DFA2	DFA3	DFA4	DFA5	DFA6	DFA7	LATCHED DATA
NOT HIGHER THAN g'	H	H	H	H	H	H	H	H
NOT HIGHER THAN f AND NOT LOWER THAN g'	L	H	H	H	H	H	H	L
NOT HIGHER THAN e' AND NOT LOWER THAN f	L	L	H	H	H	H	H	H
NOT HIGHER THAN d AND NOT LOWER THAN e'	L	L	L	H	H	H	H	L
NOT HIGHER THAN c' AND NOT LOWER THAN d	L	L	L	L	H	H	H	H
NOT HIGHER THAN b AND NOT LOWER THAN c'	L	L	L	L	L	H	H	L
NOT HIGHER THAN a' AND NOT LOWER THAN b	L	L	L	L	L	L	H	H
NOT LOWER THAN a'	L	L	L	L	L	L	L	L

FIG. 33C

READ-1st PAGE		
POTENTIAL READ OUT TO BIT LINE	DFA1	LATCHED DATA
NOT HIGHER THAN d	H	H
NOT LOWER THAN d	L	L

FIG. 34A

READ-2nd PAGE				
POTENTIAL READ OUT TO BIT LINE	DFA1	DFA2	DFA3	LATCHED DATA
NOT HIGHER THAN f'	H	H	H	H
NOT HIGHER THAN d AND NOT LOWER THAN f	L	H	H	L
NOT HIGHER THAN b AND NOT LOWER THAN d	L	L	H	H
NOT LOWER THAN b	L	L	L	L

FIG. 34B

READ-3rd PAGE								
POTENTIAL READ OUT TO BIT LINE	DFA1	DFA2	DFA3	DFA4	DFA5	DFA6	DFA7	LATCHED DATA
NOT HIGHER THAN g	H	H	H	H	H	H	H	H
NOT HIGHER THAN f AND NOT LOWER THAN g	L	H	H	H	H	H	H	L
NOT HIGHER THAN e AND NOT LOWER THAN f	L	L	H	H	H	H	H	H
NOT HIGHER THAN d AND NOT LOWER THAN e	L	L	L	H	H	H	H	L
NOT HIGHER THAN c AND NOT LOWER THAN d	L	L	L	L	H	H	H	H
NOT HIGHER THAN b AND NOT LOWER THAN c	L	L	L	L	L	H	H	L
NOT HIGHER THAN a AND NOT LOWER THAN b	L	L	L	L	L	L	H	H
NOT LOWER THAN a	L	L	L	L	L	L	L	L

FIG. 34C

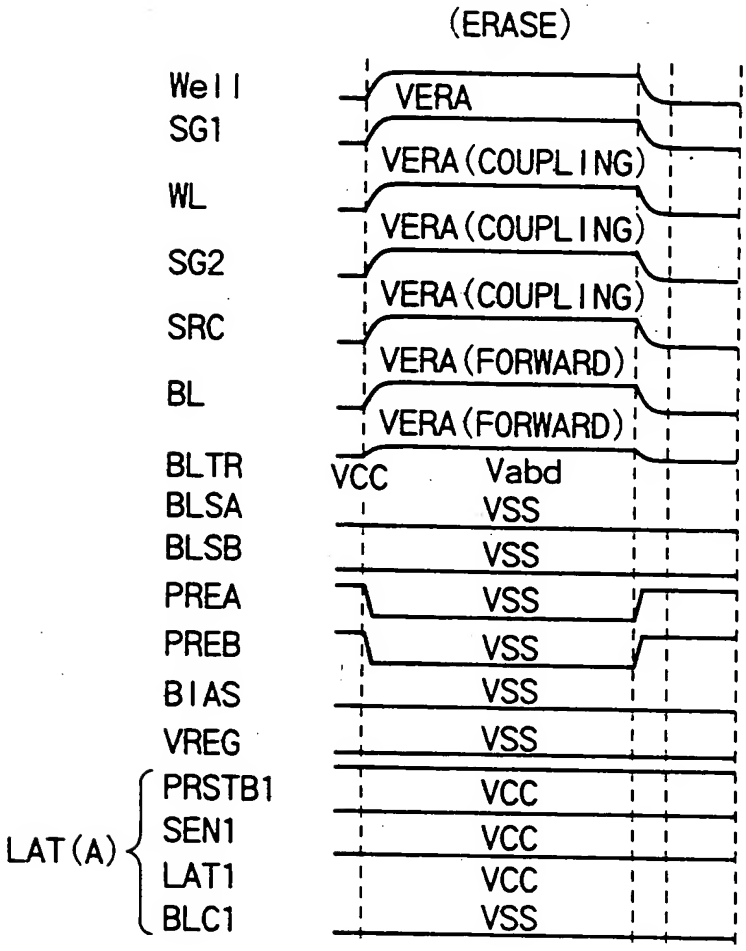

(ERASE)
Well
SG1
WL
SG2
SRC
BL
BLTR
BLSA
BLSB
PREA
PREB
BIAS
VREG
LAT(A)
PRSTB1
SEN1
LAT1
BLC1
VERA
VERA(COUPLING)
VERA(COUPLING)
VERA(COUPLING)
VERA(FORWARD)
VERA(FORWARD)
VCC
Vabd
VSS
VSS
VSS
VSS
VSS
VSS
VCC
VCC
VCC
VSS

FIG. 35

FIG. 36

MEMORY CELL DATA	MEMORY CELL THRESHOLD VALUE	EXTERNALLY INPUT DATA TO BE WRITTEN AND DATA TO BE READ			DATA OF LAT (A) BEING WRITTEN 0→A WRITE OPERATION OCCURS 1→NO WRITE OPERATION OCCURS		
		1st PAGE	2nd PAGE	3rd PAGE	1st PAGE	2nd PAGE	3rd PAGE
0	NOT HIGHER THAN 0V	1	1	1	1	1	1
1	0.3V~0.5V	1	1	0	1	1	0
2	0.8V~1.0V	1	0	0	1	0	1
3	1.3V~1.5V	1	0	1	1	0	0
4	1.8V~2.0V	0	0	1	0	1	1
5	2.3V~2.5V	0	0	0	0	1	0
6	2.8V~3.0V	0	1	0	0	0	1
7	3.3V~3.5V	0	1	1	0	0	0

FIG. 37

(2nd PAGE)

0			0→2			4			4→6			MEMORY CELL DATA
A	B	BIT	A	B	BIT	A	B	BIT	A	B	BIT	A=LAT(A), B=LAT(B), BIT=BL
H			L			L			H			EXTERNAL DATA LOADING
H		L	L		L	L		H	H		H	READ AT d
H	L	L	L	L	L	L	H	H	H	H	H	POTENTIAL OF BIT LINE IS APPLIED TO B
H	L	L	L	L	L	L	H	H	H	H	L	BIT LINE IS AT L WHEN A IS H
H	L	L	L	L	L	L	H	H	L	H	L	A IS AT L WHEN B IS AT H
H	L	H	L	L	L	L	H	H	L	H	L	BIT LINE IS AT H WHEN A IS H
H	L	H	L	L	L	H	H	H	L	H	L	POTENTIAL OF BIT LINE IS APPLIED TO A
												USE SUBSEQUENT VALUE OF A AS DATA TO BE WRITTEN

(3rd PAGE) (INTERNAL DATA CONVERSION)

0	0→1	2	2→3	4	4→5	6	6→7	MEMORY CELL DATA
A B BIT	A B BIT	A B BIT	A B BIT	A B BIT	A B BIT	A B BIT	A B BIT	A=LAT(A), B=LAT(B), BIT=BL
H	L	L	H	H	L	L	H	EXTERNAL DATA LOADING
H L	L L	L L	H L	H L	L L	L H	H H	READ AT f
H L L	L L L	L L L	H L L	H L L	L L L	L H H	H H H	POTENTIAL OF BIT LINE IS APPLIED TO B
H L L	L L L	L L L	H L L	H L H	L L H	L H H	H H L	READ AT d
H L L	L L L	L L L	H L L	H L H	L L H	L H L	H H L	BIT LINE IS AT L WHEN B IS AT H
H L L	L L L	L L L	H L L	H H H	L H H	L L L	H L L	POTENTIAL OF BIT LINE IS APPLIED TO B
H L L	L L L	L L H	H L H	H H H	L H H	L L H	H L H	READ AT b
H L L	L L L	L L H	H L H	H H L	L H L	L L H	H L H	BIT LINE IS AT H WHEN B IS AT H
H L L	L L L	L H H	H H H	H L L	L L L	L H H	H H H	POTENTIAL OF BIT LINE IS APPLIED TO B
H L L	L L L	L H H	H H L	H L L	L L L	L H H	H H L	BIT LINE IS AT L WHEN A IS AT H
H L L	L L L	L H H	L H L	H L L	L L L	L H H	L H L	A IS AT L WHEN B IS AT H
H L H	L L L	L H H	L H L	H L H	L L L	L H H	L H L	BIT LINE IS AT H WHEN A IS AT H
H L H	L L L	H H H	L H L	H L H	L L L	H H H	L H L	POTENTIAL OF BIT LINE IS APPLIED TO A
								USE SUBSEQUENT VALUE OF
								A AS DATA TO BE WRITTEN

FIG. 38

READ (1st PAGE)

0,1,2,3			4,5,6,7			MEMORY CELL DATA
A	B	BIT	A	B	BIT	A=LAT(A), B=LAT(B), BIT=BL
		L			H	01234557 AT d
L		L	H		H	BIT READ

FIG. 39A

READ (2nd PAGE)

0,1			2,3			4,5			6,7			MEMORY CELL DATA
A	B	BIT	A	B	BIT	A	B	BIT	A	B	BIT	A=LAT(A), B=LAT(B), BIT=BL
		L			L			L			H	READ AT f
L		L	L		L	L		L	H		H	POTENTIAL OF BITI LINE IS APPLIED TO A
L		L	L		H	L		H	H		H	READ AT b
L		L	L		H	L		H	H		L	BIT LINE IS AT L WHEN A IS AT H (VRFY1)
L		L	H		H	H		H	L		L	POTENTIAL OF BIT LINE IS APPLIED TO A

FIG. 39B

READ (3rd PAGE)

0		1		2		3		4		5		6		7		MEMORY CELL DATA
A	B	BIT	A	B	BIT	A	B	BIT	A	B	BIT	A	B	BIT	A	B	BIT	A=LAT(A), B=LAT(B), BIT=BL
		L			L			L			L			L			H	READ AT g
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H			POTENTIAL OF BIT LINE IS APPLIED TO A
L	L	L	L	L	L	L	L	L	L	L	H	L	H	H	H			READ AT e
L	L	L	L	L	L	L	L	L	L	L	H	L	H	H	L			BIT LINE IS AT L WHEN A IS AT H (VRFY1)
L	L	L	L	L	L	L	L	L	L	H	H	H	H	L	L			POTENTIAL OF BIT LINE IS APPLIED TO A
L	L	L	L	L	L	L	H	L	H	H	H	H	H	L	H			READ AT c
L	L	L	L	L	L	L	H	L	H	H	L	H	L	L	H			BIT LINE IS AT L WHEN A IS AT H
L	L	L	L	L	L	H	H	H	H	L	L	L	L	H	H			POTENTIAL OF BITI LINE IS APPLIED TO A
L	L	L	H	L	H	H	H	H	H	L	H	L	H	H	H			READ AT a
L	L	L	H	L	H	H	L	H	L	L	H	L	H	H	L			BIT LINE IS AT L WHEN A IS AT H (VRFY1)
L	L	H	H	H	H	L	L	L	L	H	H	H	H	L	L			POTENTIAL OF BIT LINE IS APPLIED TO A

FIG. 40

MEMORY CELL DATA	MEMORY CELL THRESHOLD VALUE	DATA TO BE WRITTEN AND READ		
		1st PAGE	2nd PAGE	3rd PAGE
0	NOT HIGHER THAN 0V	1	1	1
1	0.3V~0.5V	0	1	1
2	0.8V~1.0V	0	0	1
3	1.3V~1.5V	0	0	0
4	1.8V~2.0V	1	0	0
5	2.3V~2.5V	1	0	1
6	2.8V~3.0V	1	1	0
7	3.3V~3.5V	0	1	0

FIG. 41